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EXAMINER	
TRAN, NHAN T	
ART UNIT	**PAPER NUMBER**
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,280	ROSSI ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23,25,28-32 and 34-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23,25,28-32 and 34-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 1/21/2005 with respect to independent claims 1, 25, 31 & 34 have been fully considered but they are not persuasive.

Applicant asserts that Nair does not teach or is silent about "a readout circuit responsive to a sensed charge" as recited in claim 1, "a readout circuit comprising a charge mode amplifier" as in claim as recited in claim 31, "sensing a charge at the readout circuit" as recited in claim 25, and "a common output bus coupled to outputs of the group select circuits and to a readout circuit, the readout circuit is configured to amplify signals received from the image sensors" as recited in claim 34 (Remarks, page 12).

In response, the Examiner respectfully disagrees with the Applicant. Regarding claim 1, Nair clearly discloses in col. 4, lines 20-23 that the readout circuit (optional circuit 122 and/or signal processing pipe 126 shown in Fig. 1) is responsive to a sensed charge by further **amplifying** the image signal read out from the multiplexer 118. The above teaching of Nair also meets the limitations "a readout circuit comprising a charge mode amplifier" as recited in claim 31, "sensing a charge at the readout circuit" as recited in claim 25, and "a common output bus (e.g., the bus between multiplexer 118 and signal processing pipe 126 shown in Fig. 1) coupled to outputs of the group select circuits and to a readout circuit, the readout circuit is configured to amplify signals received from the image sensors" as recited in claim 34. Therefore, claims 1 &

25 are met by the combined teachings of Nair and Takahashi, and claims 31 & 34 are anticipated by Nair.

2. Applicant's arguments with respect to claims 16-23 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 16 & 19 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for reading out signals from **active pixel sensors** 200 of image sensor array 102, *does not* reasonably provide enablement for reading **a un-amplified pixel output signal** from each subgroup select circuit. From a technical view, each of active pixel sensors *inherently* includes a built-in amplifier (i.e., source-follower transistors). The pixel signal output from each active pixel sensor must be amplified before outputting to a column line, wherein the level of amplifying depends on bias of the transistors. Therefore, the claimed "a un-amplified pixel output signal" is NOT supported by the enablement of the active pixel sensors disclosed in the specification. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

Claims 17-18 are also rejected under 35 U.S.C. 112, first paragraph as being dependent of claim 16.

Claims 20-23 are also rejected under 35 U.S.C. 112, first paragraph as being dependent of claim 19.

Any art rejection applied to claims 16-23 below is based on best understood in view of the 112, first paragraph rejection above. It is also noted that multiple art rejections are applied to claims 16-18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Tandon et al (US 5,148,268).

Regarding claim 16, Tandon discloses a method comprising:

(a) selectively enabling a group select circuit (transistor 28 driven by ϕT2; see Fig. 5) to electrically couple a charge mode read-out amplifier (33) to a respective set of subgroup select circuits (transistors 26a-26c driven by ϕTA-ϕTC) as shown in Figs. 5 & 6; col. 4, lines 25-37 and col. 5, lines 1-15;

(b) when the group select circuit (transistor 28 driven by ϕT2; see timing diagram shown in Fig. 7B) is enabled, enabling a un-amplified pixel output signal to pass from each subgroup select circuit (transistor 26a driven by ϕTA) of the respective set of subgroup select circuits in a sequential manner (Fig. 7B shows that ϕTA, ϕTB & ϕTAC are sequentially on and off) through the group select circuit to the charge mode read-out amplifier (see Fig. 7B; col. 5, lines 30-50);

(c) subsequently disabling the group select circuit (by ϕT2) to electrically isolate the charge mode read-out amplifier from the respective set of subgroup select circuits (see timing diagram shown in Fig. 7B, wherein transistor 28 is turned off by ϕT2 after each charge from each photodiode is transferred to the amplifier 33).

Regarding claim 17, it is clear that steps (a), (b) and (c) are repeated with respect to another group select circuit and respective set of subgroup select circuits (see Fig. 7B and col. 5, lines 30-50).

Regarding claim 18, Tandon clearly discloses that the group select circuit (28) is disabled (ϕT2 becomes LOW to turn off the gate of transistor 28 as shown in Fig. 7B) after an un-amplifier pixel output signal has passed from each subgroup select circuit (26a driven by ϕTA; Fig. 7B) in the respective set of subgroup select circuits through the group select circuit to the charge mode read-out amplifier (33). See Figs. 6 & 7B.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 16 – 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Decker et al (US 6,512,546).

Regarding claim 19, Decker discloses a method comprising:

(a) selectively enabling a supergroup select circuit (5 to 1 Mux 212; Fig. 2) from a set of supergroup select circuits (a set of circuits inside 5 to 1 MUX driven by LINE_SEL_TOP [0..4] to enable selection of each line_top0 to line_top4 shown in Fig. 2) and a series-connected group select circuit (transistors CST0 & CTS5 connected to line_top0 shown in Fig. 5, similarly for CST1 & CTS 6 connected to line_top1 and so on) from an associated set of group select circuits to electrically couple a charge mode read-out amplifier (PGA 218, col. 4, lines 1-6) to a respective set of subgroup select circuits (transistors TE0, TO0,...TO329 shown in Fig. 3);

(b) when the series-connected group select circuit and supergroup select circuit are so enabled, enabling a un-amplified pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential manner (see Fig. 12A for sequential output) through the series connected group select circuit and supergroup select circuit to the charge mode readout amplifier (see Figs. 11& 12; col. 13, lines 20-41).

(c) disabling the group select circuit to electrically isolate the charge mode read-out amplifier from the respective set of subgroup select circuits (see Figs. 11 & 12 and col. 13, lines 20-41, wherein the group select circuits CST0-CST329 are sequentially turned on and off to sequentially isolate columns TCRL0-TCRL329 from outputting signals to the amplifier 218 right after each of them was read out).

It is importantly noted that the supergroup select circuits are taken as the set of circuits inside of the TOP 5 to 1 MUX 212 only.

Regarding claim 20, see the analysis of claim 19 for the same operations with respect to another series-connect group associated with the supergroup select circuit and a respective set of subgroup select circuits for the imaging device to function as disclosed.

Regarding claim 21, see the analysis of claim 19.

Regarding claims 22 & 23, also see the analysis of claim 19, wherein disabling the supergroup select circuit occurs after a pixel output signal has passed from each subgroup select circuit in the respective sets of subgroup select circuits associated with each of the group select circuits through the supergroup select circuit and to the charge mode read-out amplifier. See Fig. 12.

Regarding claims 16-18, see the analyses of claims 19-21.

5. Claims 31, 32 & 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Nair et al (US 6,366,320).

Regarding claim 31, Nair discloses an imager device (Figs. 1 & 7) comprising:

groups of image sensors (one group corresponds to multiple columns of sensors selected by each multiplexer 130 to 179 of a first level multiplexing), each comprising a plurality of columns of an image sensor array (col. 3, lines 48-56 and col. 5, line 59 – col. 6, line 15);

a plurality of column select circuits (gate pairs in first level muxes 130-179), each of which is coupled to an output from a column of sensors (see Fig. 1);

a plurality of group select circuits (gate pairs in muxes 180-186), each of which is coupled via a first bus (e.g., a bus between 130 and 180) to outputs from the column select circuits (Fig. 1);

a readout circuit (122 and/or 126) connected to outputs of said group select circuits (via mux 187), the readout circuit comprising a charge mode amplifier (col. 4, lines 20-22);

a controller (192) for providing control signals to the column select circuits and the group select circuits so selectively enable the respective column select circuits and group select circuits to pass signals from the sensors to said readout circuit one sensor at a time (see Fig. 1, col. 3, line 48 – col. 4, line 25, wherein image signal is sequentially output to readout circuit 122/126 pixel by pixel at the output of multiplexer 118).

Regarding claim 32, Nair also refers that the image sensors are active pixel sensors (col. 1, lines 16-20).

Regarding claim 34, Nair discloses an imager device comprising:

an array of image sensors organized into supergroups (selected by each gate pair in mux 187) comprising groups (selected by gate pairs in muxes 180-186) of subgroups (selected by gate pairs in muxes 130-179) of image sensors (see Figs. 1 & 7; col. 3, lines 48-56 and col. 5, line 59 – col. 6, line 15);

subgroup select circuits (gate pairs in muxes 130-179), each of which is coupled to outputs of the sensors of a respective subgroup; group select circuits (gate pairs in muxes 180-186), each of which is coupled to outputs of subgroup select circuits associated with a respective one of the groups (Fig. 1);

supergroup select circuits (each gate pair in mux 187), each of which is coupled to outputs of group select circuits associated with a respective one of the supergroups (Fig. 1);

at least two group buses (buses between muxes 130-179 and 180-186), each of group bus coupled to output of the subgroup select circuits associated with a respective group (Fig. 1);

a common output bus (an output bus between 187 and 126) coupled to outputs of the groups select circuits (via mux 187) and to a readout circuit (122 and/or 126), the readout circuit is configured to amplify signals received from the image sensors (see Fig. 1; col. 4, lines 20-22);

a controller (192) for providing control signals to the image sensors to produce a readout signal and to the supergroup select circuits, group select circuits and subgroup select circuits to selectively enable the respective supergroup, group and subgroup select circuits to pass output signals from the image sensors to the readout circuit one sensor at a time (see col. 3, line 48 –

col. 4, line 25, wherein image signal is sequentially output to readout circuit 122/126 pixel by pixel at the output of multiplexer 118).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-15, 25, 28-30 & 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair et al (US 6,366,320) in view of Takahashi et al (US 4,551,634).

Regarding claim 1, Nair discloses an apparatus comprising:

groups of image sensors (one group corresponds to each multiplexer 130 to 179 of a first level multiplexing), each group comprising subgroups (columns) of sensors (see Figs. 1 & 7; col. 1, lines 10-29; col. 3, lines 48-56; col. 5, line 59 – col. 6, line 15);

subgroup select circuits (gate pairs in multiplexers 130 to 179), each of which is coupled to outputs from a respective subgroup of sensors (see Fig. 1; col. 3, lines 44-56);

group select circuits (gate pairs in multiplexers 180 to 186), each of which is coupled to outputs from subgroup select circuits associated with a respective one of the groups (Fig. 1);

a first bus for each group coupled to the outputs of the associated subgroup select circuits (i.e., a bus between 130 and 180; Fig. 1);

a common output bus (i.e., the bus at the output of multiplexer 118) for receiving signals from each of the groups, the common output bus connected to a readout circuit (122 and/or 126), the readout circuit responsive to a sensed charge (col. 4, lines 20-22, 40-43):

a controller (192) for providing control signals to the subgroup select circuits and the group select circuits to selectively enable the respective subgroup select circuits and group select circuits to pass signals from the sensors to a readout circuit (122, 126) one sensor at a time (sequential outputting/multiplexing of pixel by pixel, column by column) as shown in Fig. 1; col. 3, line 48 – col. 4, line 25;

a first isolation circuit (each gate pair in multiplexers 180 to 186) coupled to each first bus for selectively isolating each group from the readout circuit (e.g., turning on and then off each gate pair of multiplexers 180 to 186 in column by column basis). See Fig. 1; col. 3, line 48 – col. 4, line 25.

Nair fails to explicitly teach that the first isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage. Takahashi teaches a multiplexing circuit in which a third transistor (23-x) is added in addition to a pair of transistors (21-x and 22-x) to clamp the voltage level of each non-selected channel (isolated bus) to ground so that mutual interference such as noise, crosstalk between neighboring selected and non-selected channels are prevented. See Takahashi, Fig. 2, col. 1, lines 45-55 and col. 3, line 15 – col. 4, line 15.

Therefore, it would have been obvious to one of ordinary skill in the art to improve signal integrity of the analog multiplexer 118 in Nair by implementing a switch (i.e., a transistor) in the

first isolation circuit for selectively connecting the first bus to a predetermined voltage (i.e., 0V ground) to eliminate mutual interference between neighboring buses in view of the teaching of Takahashi.

Regarding claim 2, Nair also refers that the sensors are active pixel sensors (col. 1, lines 16-20).

Regarding claim 3, Nair further discloses a second bus coupled to the outputs of the group select circuits and the readout circuit (i.e., a bus between 180 and 187 that is coupled to the readout circuit 122, 126 via 187).

Regarding claim 4, Nair discloses that the number of group select circuits is approximately equal to the square root of the number of the subgroup select circuits (col. 4, lines 3-10, wherein 7 second level muxes $\cong$ square root of 50 first level muxes).

Regarding claims 5 & 6, although Nair and Takahashi do not specifically disclose that a ratio of the number of subgroup select circuits to group select circuit is in a range of 15:1 and 30:1 as required in claim 6 (this is also within the range of 10:1 and 40:1 required in claim 5), Nair suggests, in col. 1, lines 29-37, that modern imaging arrays can be very large and future arrays are expected to be even larger which requires modification on circuit design. Therefore, it would have been obvious to one of ordinary skill in the art to implement a ratio of the number of

subgroup select circuits to group select circuit in a range of 10:1 and 15:1 as an obvious design variation depending on a size of an image sensor to balance readout speed.

Regarding claim 7, in col. 4, lines 3-10 and Fig. 1, Nair discloses that the 32 predetermined coded lines selects one of 16 pass gate pairs in the selected first level mux, a corresponding one of 8 pass gate pairs in the selected second level mux, and finally a corresponding one of 8 pass gate pairs in the third level mux. It is implied that when one gate pair in the multiplexer 180 corresponding to the 16 gate pairs in the multiplexer 130 is **ON**, the 16 gate pairs are also sequentially **ON** to pass the signals from the 16 gate pairs to the first bus between the 130 and 180 for the multiplexers sequentially output signals. When the signals output from the 16 gate pairs are done, the corresponding gate pair in the multiplexer 180 must be **OFF** and a next gate pair of the 8 gate pairs in the multiplexer 180 is **ON** to sequentially receives output signals from the next corresponding 16 gate pairs (i.e., 131) and so on. Thus, each group select circuit of 180 comprises at least a transistor switch with a respective gate terminal (either a full CMOS gate or a half gate) for receiving a control signal from the controller (192), wherein when the switch is turned on, the group select circuit is enabled to pass signals from associated subgroup select circuits to the first bus, and when the switch is turned off, the group select circuit is disabled from passing signals from the associated group select circuits to the first bus.

Regarding claim 8, see the analysis in claim 7 for the similar structure and operations of each subgroup select circuit.

Regarding claim 9, Nair discloses that the controller (192) is configured for generating the control signals (by decoding 10 bit column address) to enable and disable the group select circuit switches and the subgroup select circuit switches in a predetermined sequence (col. 3; line 57 – col. 4, line 10 and note that a predetermined sequence is pixel by pixel in column by column basis as described in col. 3, lines 42-46).

Regarding claim 10, Nair also discloses that the controller is configured to provide the control signals to enable the switches in the group select circuits sequentially, and, while a particular group select switch is enabled, to enable the subgroup select circuits associated with the particular group select circuit sequentially, one at a time (Fig. 1; col. 4, lines 3-10 and the Examiner's analysis in claims 1, 7 & 9 are also applied here).

Regarding claim 11, see the analysis in claim 9.

Regarding claim 12, although Nair and Takahashi do not specifically disclose that each group select circuit comprises a pair of NMOS transistor switches, Nair suggests that each pair can be a full CMOS transmission gate (comprises a complementary pair of a NMOS and a PMOS transistor), a half gate (either a pair of PMOS transistors or a pair of NMOS transistors) or any other device that acts as a switch (col. 3, lines 52-56).

Therefore, it would have been obvious to one of ordinary skill in the art to implement the switches by using NMOS switches instead of a full CMOS switches in view of the suggestion of

Nair in an obvious configuration for the transmission gates. *It should be noted that the third transistor taught in Takahashi is not considered as a transmission gate. It is simply a switch to ground.*

Regarding claim 13, Nair further discloses supergroups of sensors (all sensors that correspond to *each* of multiplexers 180 to 186; Fig. 1);

supergroup select circuits (gate pairs in multiplexer 187), each of which is coupled to outputs from group select circuits associated with respective one of the supergroups;

a second isolation circuit (also, gate pairs in multiplexer 187) coupled to each second bus (i.e., a bus between 180 and 187) for selectively isolating each supergroup from the readout circuit;

wherein the controller is configured to provide control signals to the supergroup select circuits to selectively enable a supergroup select circuit to pass a signal from the second bus to a third bus (i.e., a bus between 187 and 126) which is a common output bus (see Fig. 1 and the Examiner's analysis in claims 1, 3, 7 & 9).

Although Nair does not teach the second isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage, a similar motivation and modification as expressed in claim 1 is further applied to the second isolation circuit in view of the teaching of Takahashi to maintain signal integrity throughout the multiplexer 118.

Regarding claim 14, it is shown by Nair, Fig. 1 at multiplexer 187 that an output of each supergroup select circuit is electrically coupled to a common output bus.

Regarding claim 15, see claim 7 for the similar analysis for a transistor switch with a respective gate terminal for receiving a control signal from the controller.

Regarding claim 25, see the analysis of the apparatus claim 1, wherein sensing a charge at the readout circuit is further disclosed by Nair, col. 4, lines 20-22. It is also noted that the subgroup select circuit allows a signal from each sensor in the subgroup to pass sequentially to a readout circuit electrically coupled to the group select circuit in order for the multiplexing 118 to function as disclosed in col. 4, lines 3-10.

Regarding claim 28, see the analysis of claim 13.

Regarding claim 29, Nair clearly discloses a step of coupling each supergroup select circuit (gate pairs in multiplexer 187) to an associated second bus (i.e., a bus between 180 and 187), wherein the readout signals from each sensor in the supergroup inherently travel through the second bus as shown Fig. 1 and col. 3, lines 48-56.

Regarding claim 30, see the analysis of claim 13.

Regarding claims 35 & 36, as clearly taught by Takahashi, the predetermined voltage is a ground potential. See Takahashi, col. 3, lines 49-52 and col. 4, lines 10-15.

Regarding claim 37, it is also disclosed by Nair that the common output bus is connected between outputs from the group select circuits (via mux 187) and the readout circuit (Fig. 1).

Regarding claim 38, it is also disclosed by Nair that common output bus is connected between the outputs from the supergroup select circuits and readout circuit (Fig. 1).

Regarding claim 39, see the analysis of claim 1.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

DAVID L. OMETZ
PRIMARY EXAMINER